cofc
EW

ATTORNEY'S DOCKET NO.: S1022.80707US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ferruccio Frisina		
Serial No.:	09/925,080	Patent No. 6,809,383 B2	
Filed:	August 8, 2001	Issued: October 26, 2004	
For:	METHOD OF MANUFACTURING AN INTEGRATED EDGE STRUCTURE FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES, AND RELATED INTEGRATED EDGE STRUCTURE		
Examiner:	Chuong A.Luu		
Art Unit:	2825	Confirmation No.:	3073

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.323

Sir/Madam:

Patentees respectfully request the correction of errors in the above-captioned patent. Specifically, the there are errors in claims 26-28 of issued U.S. Patent No. 6,809,383 B2.

Claims 25-28 of issued U.S. Patent No. 6,809,383 are not the same as the claims as filed in the amendment filed on December 15, 2003. Applicant has reproduced below the claims of U.S. Patent No. 6,809,383 showing the terminology of the claims as allowed with insertions indicated by underlining and terminology inserted at the time of printing indicated by strikeouts.

26. An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases curvature radii of equipotential lines associated with ~~a breakdown voltage of~~ the edge portion of the depletion region.

27. An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure decreases an electric field associated with ~~increases a breakdown voltage of~~ the edge portion of the deletion layer ~~depletion region~~.

28. An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion and a plane portion, and

wherein the edge structure reduces a ratio of ~~increases~~ a breakdown voltage of the edge portion to a breakdown voltage of plane portion.

There was no amendment made by either the Examiner or Patentee making the above changes to the application.

In support of this Request Patentees enclose highlighted copies of the amendment filed on December 15, 2003 and column 8 of issued U.S. Patent No. 6,809,383. Also enclosed is PTO form SB/44.

Please issue a Certificate of Correction in U.S. Letters Patent No. 6,809,383 as specified on the attached Certificate.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Patentee respectfully submits that, since the errors for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Correspondence and Mail Division, Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 3rd day of October, 2005.

Attorney Docket No.: S1022.80707US00
XNDD

Respectfully submitted,

Ferruccio Frisina, Applicant

By: _____

James H. Morris, Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 646-8000

ATTORNEY'S DOCKET NO: S1022.80707US00
(formerly S01022.80707.US)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ferruccio Frisina
Serial No.:	09/925,080
Filed:	August 8, 2001
For:	METHOD OF MANUFACTURING AN INTEGRATED EDGE STRUCTURE FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES, AND RELATED INTEGRATED EDGE STRUCTURE
Confirmation No.:	3073
Examiner:	Luu, Chuong A.
Art Unit:	2825

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first- class postage attached, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 15, 2003.

Jeanne Spinelli

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action mailed July 14, 2003, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the Listing of Claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

In the Claims

Applicant has submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Listing of the Claims

1-12. (Cancelled).

13. (Currently Amended) An integrated edge structure for a high voltage semiconductor device, comprising a number of superimposed semiconductor layers of a first conductivity type and at least two columns of doped regions of a second conductivity type, said columns disposed in said number of superimposed semiconductor layers, wherein, for each column of the at least two columns, the column is deeper than each column of the at least two columns that is farther from said high voltage semiconductor device than the column, and wherein each of the at least two columns is spaced from any other of the at least two columns.

14. (Original) The integrated edge structure according to claim 13, wherein said high voltage semiconductor device is a power MOSFET.

15. (Previously Presented) The integrated edge structure according to claim 13, wherein said number of superimposed semiconductor layers is superimposed on a semiconductor substrate.

16. (Previously Presented) The integrated edge structure according to claim 13, wherein each one of said at least two columns has a depth decreasing by shifting from said high voltage semiconductor device towards an outside of the integrated edge structure.

17. (Original) The integrated edge structure according to claim 13, wherein the doped regions of each one of said at least two columns are superimposed and vertically merged to each other.

18. (Original) The integrated edge structure according to claim 13, wherein the doped regions of each of said at least two columns are superimposed but not merged to each other.

19. (Previously Presented) The integrated edge structure according to claim 13, wherein said first conductivity type is N type and said second conductivity type is P type.

20. (Previously Presented) The integrated edge structure according to claim 13, wherein said first conductivity type is P type and said second conductivity type of conductivity is N type.

21. (Previously Presented) The integrated edge structure according to claim 13, wherein one or more doped regions of the at least two columns has a dopant concentration of approximately $1x10^{15}$ atoms/cm^2 or less.

22. (Previously Presented) The integrated edge structure according to claim 13, wherein the number of superimposed semiconductor layers have a similar dopant concentration.

23. (Previously Presented) The integrated edge structure according to claim 13, wherein the number of superimposed semiconductor layers have a similar thickness.

24. (Cancelled).

25. (Currently Amended) An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed, and

wherein the edge structure further comprises a plurality of layers of a second conductivity type superimposed on one another, wherein each region of the plurality of regions is disposed within at least two of the plurality of superimposed layers.

26. (Previously Presented) The edge structure of claim 25, wherein each sub-region of each region is a doped semiconductor.

27. (Previously Presented) The edge structure of claim 26, wherein each of the plurality of sub-regions of the plurality of regions has a dopant concentration of approximately $1x10^{15}$ atoms/cm^2 or less.

28. (Cancelled).

29. (Currently Amended) The edge structure of claim ~~28~~ 25, wherein each region of the plurality of regions is spaced from each of the other of the plurality of regions by portions of two or more of the plurality of superimposed layers.

30. (Currently Amended) The edge structure of claim ~~28~~ 25, wherein the plurality of superimposed layers is superimposed on a semiconductor substrate.

31. (Currently Amended) The edge structure of claim ~~28~~ 25, wherein the plurality of superimposed layers have a similar dopant concentration.

32. (Currently Amended) The edge structure of claim ~~28~~ 25, wherein the plurality of superimposed layers have a similar thickness.

33. (Previously Presented) The edge structure of claim 25, wherein the semiconductor device is a high-voltage semiconductor device.

34. (Previously Presented) The edge structure of claim 33, wherein the semiconductor device is a power MOSFET.

(Previously Presented) The edge structure of claim 25, wherein, for one or more of the plurality of regions, the plurality of superimposed sub-regions are merged together.

35. (Previously Presented) The edge structure of claim 25, wherein, for one or more of the plurality of regions, the plurality of superimposed sub-regions are not merged together.

36. (Previously Presented) The edge structure of claim 25, wherein the first conductivity type is N type and the second conductivity type is P type.

37. (Previously Presented) The edge structure of claim 25, wherein the first conductivity type is P type and the second conductivity type is N type.

38. (Currently Amended) ~~The edge structure of claim 25,~~ An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases a breakdown voltage of the edge portion of the depletion region.

39. (Currently Amended) ~~The edge structure of claim 25,~~ An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions,

each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases curvature radii of equipotential lines associated with the edge portion of the depletion region.

40. (Currently Amended) ~~The edge structure of claim 25,~~ An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure decreases an electric field associated with the edge portion of the deletion layer.

41. (Currently Amended) ~~The edge structure of claim 25,~~ An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each

region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion and a plane portion, and

wherein the edge structure reduces a ratio of a breakdown voltage of the edge portion to a breakdown voltage of plane portion.

REMARKS

In response to the Office Action mailed July 14, 2003, the Applicant respectfully requests reconsideration.

To further the prosecution of this application, amendments have been made in the claims, as illustrated above, under the sub-heading *Listing of the Claims*.

Claims 1-42 were previously pending in this application. By this amendment, Applicant cancels claims 24 and 28 without prejudice or disclaimer, and amends claims 13, 25, 29-32 and 39-42. As a result, claims 13-23, 25-27 and 29-42 are pending for examination, of which claims 13, 25 and 39-42 are independent.

1. Claims 13-23 Are In Condition For Allowance

Claims 13-23 stand rejected under 35 U.S.C. §103(a) as purportedly being unpatentable over U.S. Patent No. 6,225,165 (Noble) in view of U.S. Patent No. 5,719,411 (Ajit). Further, the Office Action states that claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Although Applicant believes that claim 13 patentably distinguishes over Nobel in view of Ajit, Applicant has amended claim 13 to avoid further delay in the prosecution of this application. Specifically, Applicant has amended claim 13 (i.e., the base claim) as shown above to include all of the limitations of claim 24 (it should be appreciated that there are no intervening claims between claim 13 and claim 24). Accordingly, Applicant respectfully submits that claim 13, as amended, patentably distinguishes over Noble in view of Ajit, and respectfully submits that the rejection of claim 13 under §103(a) be withdrawn.

Claims 14-23, which each depends directly or indirectly from independent claim 13, patentably distinguish over Noble in view of Ajit for at least the same reasons as discussed above with respect to claim 13. Accordingly, Applicant respectfully requests that the rejection of claims 14-23 under §103(a) be withdrawn.

2. Claims 25-27 and 29-42 Are In Condition For Allowance

Claims 25-27 and 33-38 stand rejected under 35 U.S.C. §103(a) as purportedly being unpatentable over Noble in view of Ajit. Further, claims 28-32 and 29-42 stand objected to as

being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Although Applicant believes that claim 25 patentably distinguishes over Nobel in view of Ajit, Applicant has amended claim 25 to avoid further delay in the prosecution of this application. Specifically6, Applicant has amended claim 25 (i.e., the base claim) to include all of the limitations of claim 28. Further, Applicant has amended claims 29-32 to recite dependency from claim 25 as opposed to claim 28. Applicant also has amended each of claims 39-42 to include all of the limitations of independent claim 25 (i.e., the base claim).

Accordingly, Applicant respectfully submits that claims 25 and 39-42, as amended, patentably distinguish over Noble in view of Ajit, and requests that the rejection of these claims under §103(a) be withdrawn. Claims 26, 27 and 29-38, which each depend directly or indirectly from independent claim 25, patentably distinguish over Noble in view of Ajit for at least the same reasons as set forth above with respect to claim 25. Accordingly, Applicant respectfully requests that the rejection of these claims under §103(a) be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee

occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted
Ferruccio Frisina, Applicant

By: _____

Daniel P. McLoughlin, Reg. No. 46, 066
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2211
Tel. No.: (617) 720-3500
Attorney for Applicant

Docket No.: S1022.80707US00
(formerly S01022.80707.US)
Date: December 15, 2003
x12/15/03x

ATTORNEY'S DOCKET NO.: S1022.80707US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ferruccio Frisina	
Serial No.:	09/925,080	Patent No. 6,809,383 B2
Filed:	August 8, 2001	Issued: October 26, 2004
For:	METHOD OF MANUFACTURING AN INTEGRATED EDGE STRUCTURE FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES, AND RELATED INTEGRATED EDGE STRUCTURE	

Examiner: Chuong A.Luu
Art Unit: 2825 Confirmation No.: 3073

Correspondence and Mail Division
Certificate of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of: 12/15/03 Amend and Col 8 of U.S. Patent No. 6,809,383
[X] PTO Form SB/44
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 646.8000 , Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Correspondence and Mail Division, Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 3rd day of October , 2005.

Attorney Docket No.: S1022.80707US00
XNDD

Respectfully submitted,

Ferruccio Frisina, Applicant

By:

James H. Morris, Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 646-8000

PTO/SB/44 (04-04)
Approved for use through 04/30/2007
U.S. Patent and Trademark Office; US. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	:	6,809,383
DATED	:	October 26, 2004
INVENTOR(S)	:	Ferruccio Frisina

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 26, col. 8, line 5 should read:
--wherein the edge structure increases curvature radii of equipotential lines associated with--

Claim 27, col. 8, line 27-28 should read:
--wherein the edge structure decreases an electric field associated with the edge portion of the deletion layer.--

Claim 28, col. 8, line 49-50 should read:
--edge portion and a plane portion, and
wherein the edge structure reduces a ratio of a breakdown voltage--

MAILING ADDRESS OF SENDER

PATENT NO. 6,809,383

James H. Morris
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210

19. The edge structure of claim 12, wherein the semiconductor device is a high-voltage semiconductor device.

20. The edge structure of claim 19, wherein the semiconductor device is a power MOSFET.

21. The edge structure of claim 12, wherein, for one or more of the plurality of regions, the plurality of superimposed sub-regions are merged together.

22. The edge structure of claim 12, wherein, for one or more of the plurality of regions, the plurality of superimposed sub-regions are not merged together.

23. The edge structure of claim 12, wherein the first conductivity type is N type and the second conductivity type is P type.

24. The edge structure of claim 12, wherein the first conductivity type is P type and the second conductivity type is N type.

25. An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases a breakdown voltage of the edge portion of the depletion region.

26. An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases a breakdown voltage of the edge portion of the depletion region.

27. An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases a breakdown voltage of the edge portion of the depletion region.

28. An edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising:

a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, each region laterally spaced from any other regions of the plurality of regions, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit,

wherein, for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed,

wherein the semiconductor device includes a PN junction having an associated depletion region including an edge portion, and

wherein the edge structure increases a breakdown voltage of the edge portion to a breakdown voltage of plane portion.

* * * * *